REMARKS

In the June 6, 2006 Office Action, the Examiner rejected pending claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by U. S. Patent Publication No. 2004/0198420 to He et al. (hereinafter "He"). Applicants respectfully traverse the rejection and request that pending claims 1-20 be allowed for the reasons set forth herein.

A. Claims 1-20 Are Not Anticipated

In response to the Examiner's rejection of claims 1-20 as being anticipated by the He Publication, Applicants respectfully request reconsideration of the rejection in view of the amendments and remarks presented herein.

As variously described and claimed in each of the independent claims, Applicants have disclosed a scheme for sharing an antenna control pin set between first and second wireless transceiver circuits, each of which is coupled to its own plurality of antennas. By providing a routing circuit for coupling antenna control signals to the shared antenna control pin set, the antenna control signal is routed to the appropriate wireless transceiver circuitry in a multi-transceiver system using a minimum number of pins, *thereby allowing signal transmission/reception to occur at whichever antenna set is associated with the selected wireless transceiver circuit.*

This is nowhere disclosed or suggested in the referenced disclosure (Figure 1 and paragraphs 19-25) from the He Publication which describes sharing a single set of antennas between multiple transceiver circuits. In particular, the He Publication depicts a dual-mode (IEEE 802.11a/b) WLAN module which transmits and receives both 802.11a and 802.11a signals over a single shared set of dual-band antennas 43a, 43b. *See*, He Publication, paragraph 19. Indeed, while the Examiner appears to identify He's "Antenna_Control" signal that is supplied to the switch SW1 as corresponding to the claimed first antenna control signal, the Examiner has not identified a second antenna control signal that is generated at a shared pin set for use in controlling receiving or transmitting operations over a second plurality of antennas coupled to a second wireless transceiver circuit as variously claimed herein. *See*, Office Action dated June 6, 2006, pp. 2-3. For that matter, He's "Antenna_Control" signal is only used to switch between the two antennas 43a, 43b, and does not control which wireless transceiver circuit receives or transmits a communication packet. At best, the He Publication discloses a dual-mode radio frequency front end circuit 4 in which a first transceiver circuit (41a, 42a) and a second transceiver circuit (41b, 42b) both transmit and receive over a single set of shared

antennas (43a, 43b). Because there is only a single set of antennas (43a, 43b) shared between the two transceiver circuits, the He Publication entirely fails to disclose that an antenna control signal is routed over a shared pin set to either a first wireless transceiver circuit (having its own plurality of antennas) or a second wireless transceiver circuit (having its own plurality of antennas).

In addition to the missing requirements from the independent claims, Applicants respectfully submit that there are numerous missing requirements from the dependent claims. For example, there is no disclosure in the He Publication of an 802.11g radio transceiver circuit (as variously recited in claims 2, 12, 13 and 19) since the passages referenced by the Examiner refer only to a dual-mode 802.11a/b WLAN module. As for the multiplexer requirement variously recited in claims 3, 15 and 19 for selecting between two antenna control signals for routing to a shared pin set, the Examiner has failed to identify any corresponding multiplexer disclosure in the He Publication,[1] and Applicants respectfully submit that there is none. As for the rejection[2] of claims 6 and 7, there is no disclosure in the He Publication of a PHY module which generates first and second antenna control signals, since the Examiner has referenced only a single "Antenna_Control" signal being generated by the dual-mode baseband integrated circuit 2. Likewise, the Examiner's rejection of the integrating a PHY module and transceiver circuit on a single chip (as recited in claim 7)[3] is directly refuted by He's disclosure that the baseband processor is implemented on one chip (the BBIC 2), the dual-mode radio frequency integrated circuit is implemented on a second chip (RFIC 3) and the radio frequency front-end circuit is implemented with discrete circuitry (RF front end circuit 4). *See*, He Publication, Abstract and paragraph 14. Similarly, the single chip requirement of claim 8 is likewise directly refuted by the disclosure of the He Publication, which uses a combination of discrete circuitry (RF front end

[1] While the Examiner purports to reject a "multiplexer" requirement in claims 3 and 13, Applicants respectfully submit that this requirement is explicitly set forth in claims 3, 15 and 19, and submit this response accordingly.

[2] While the Examiner purports to reject a requirement in claims 6 and 16 of "PHY module" for generating first and second antenna control signals, Applicants respectfully submit that this requirement is explicitly set forth in claims 6 and 7, and submit this response accordingly.

[3] While the Examiner purports to reject a requirement in claims 7 and 17 of integrating a "PHY module" and "first wireless transceiver circuit" on a single chip, Applicants respectfully submit that this requirement is explicitly set forth in claim 7, and submit this response accordingly.

circuit 4) and multiple chips (RFIC 3 and BBIC 2).[4] As for the rejection of claims 9 and 10 (which variously recite a second wireless transceiver circuit having its own antennas being controlled by a second antenna control signal), Applicant's submit that these requirements are wholly missing from the disclosure of the He Publication which discloses only a single set of shared antennas (43a, 43b). Finally, claim 20 has been rejected without any apparent analysis of the claim requirement. *See*, Office Action, pp. 4-5. Applicants respectfully submit that the recitation in claim 20 (of implementing the baseband processing module, first front end modulator and second front end modulator as separate integrated circuits) is directly refuted by the disclosure of the He Publication, which uses a combination of discrete circuitry (RF front end circuit 4) and multiple chips (RFIC 3 and BBIC 2).

In view of the amendments and remarks set forth herein, Applicants respectfully submit that all pending claims are in condition for allowance. Accordingly, Applicants request that the rejection of claims 1-20 be withdrawn and that a Notice of Allowance be issued. If there are any remaining issues that might be resolved through a telephonic interview, Applicants' undersigned representative would welcome an opportunity to discuss such issues with the Examiner.

FILED ELECTRONICALLY

September 29, 2006

Respectfully submitted,

/Michael Rocco Cannatti/

Michael Rocco Cannatti
Attorney for Applicants
Reg. No. 34,791

[4] While the Examiner purports to reject a requirement in claims 8 and 18 of forming the second wireless transceiver circuit on a single chip, Applicants respectfully submit that this requirement is explicitly set forth in claim 8, and submit this response accordingly.